Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 120 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
- Non-Volatile Program and Data Memories
  - 2/4/8K Bytes of In-System Programmable Program Memory Flash
    - Endurance: 10,000 Write/Erase Cycles
  - 128/256/512 Bytes of In-System Programmable EEPROM
    - Endurance: 100,000 Write/Erase Cycles
  - 128/256/512 Bytes of Internal SRAM
  - Data retention: 20 years at 85°C / 100 years at 25°C
  - Programming Lock for Self-Programming Flash & EEPROM Data Security
- Peripheral Features
  - One 8-Bit and One 16-Bit Timer/Counter with Two PWM Channels, Each
  - 10-bit ADC
    - 8 Single-Ended Channels
    - 12 Differential ADC Channel Pairs with Programmable Gain (1x / 20x)
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-Chip Analog Comparator
  - Universal Serial Interface
- Special Microcontroller Features
  - debugWIRE On-chip Debug System
  - In-System Programmable via SPI Port
  - Internal and External Interrupt Sources: Pin Change Interrupt on 12 Pins
  - Low Power Idle, ADC Noise Reduction, Standby and Power-Down Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-Out Detection Circuit
  - Internal Calibrated Oscillator
  - On-Chip Temperature Sensor
- I/O and Packages
  - Available in 20-Pin QFN/MLF & 14-Pin SOIC and PDIP
  - Twelve Programmable I/O Lines
- Operating Voltage:
  - 1.8 – 5.5V for ATtiny24V/44V/84V
  - 2.7 – 5.5V for ATtiny24/44/84
- Speed Grade
  - ATtiny24V/44V/84V
    - 0 – 4 MHz @ 1.8 – 5.5V
    - 0 – 10 MHz @ 2.7 – 5.5V
  - ATtiny24/44/84
    - 0 – 10 MHz @ 2.7 – 5.5V
    - 0 – 20 MHz @ 4.5 – 5.5V
- Industrial Temperature Range: -40°C to +85°C
- Low Power Consumption
  - Active Mode (1 MHz System Clock): 300 µA @ 1.8V
  - Power-down Mode: 0.1 µA @ 1.8V

8-bit AVR® Microcontroller with 2/4/8K Bytes In-System Programmable Flash

ATtiny24/44/84

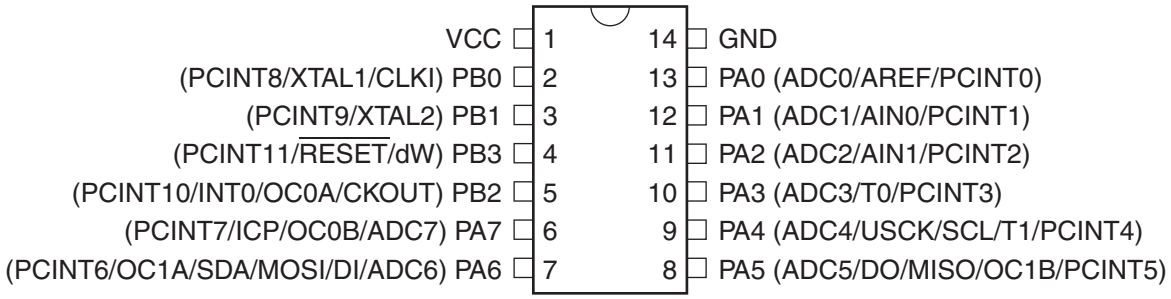
Preliminary Summary

Rev. 8006GS–AVR–01/08

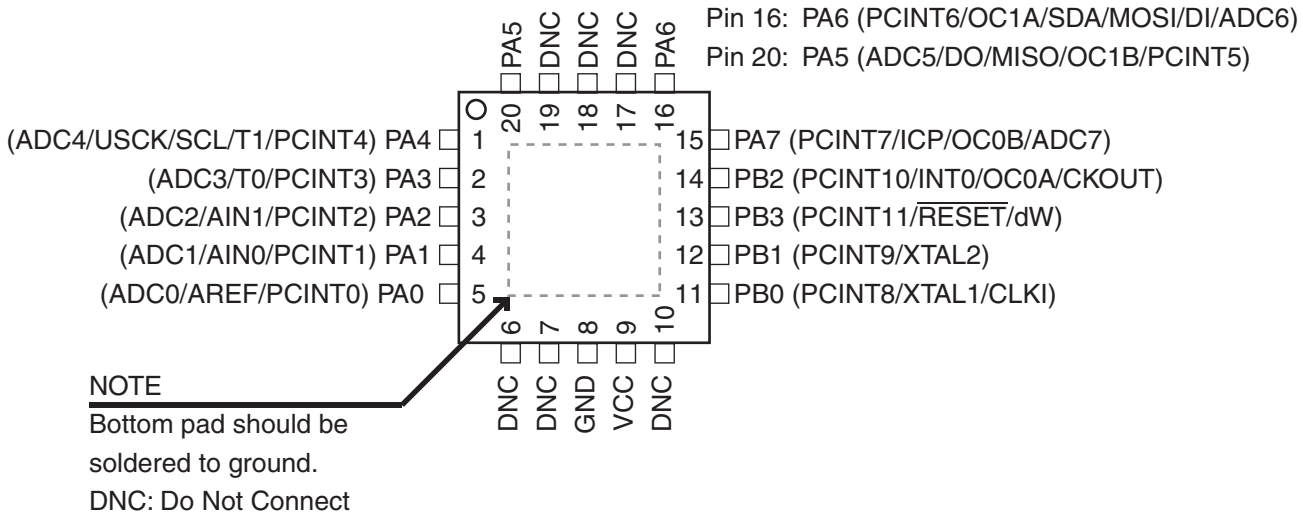
1. Pin Configurations

Figure 1-1. Pinout ATtiny24/44/84

PDIP/SOIC



QFN/MLF



1.1 Pin Descriptions

1.1.1 VCC

Supply voltage.

1.1.2 GND

Ground.

1.1.3 Port B (PB3...PB0)

Port B is a 4-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability except PB3 which has the $\overline{\text{RESET}}$ capability. To use pin PB3 as an I/O pin, instead of RESET pin, program (‘0’) RSTDISBL fuse. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features.

1.1.4 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided the reset pin has not been disabled. Shorter pulses are not guaranteed to generate a reset.

The reset pin can also be used as a (weak) I/O pin.

1.1.5 Port A (PA7...PA0)

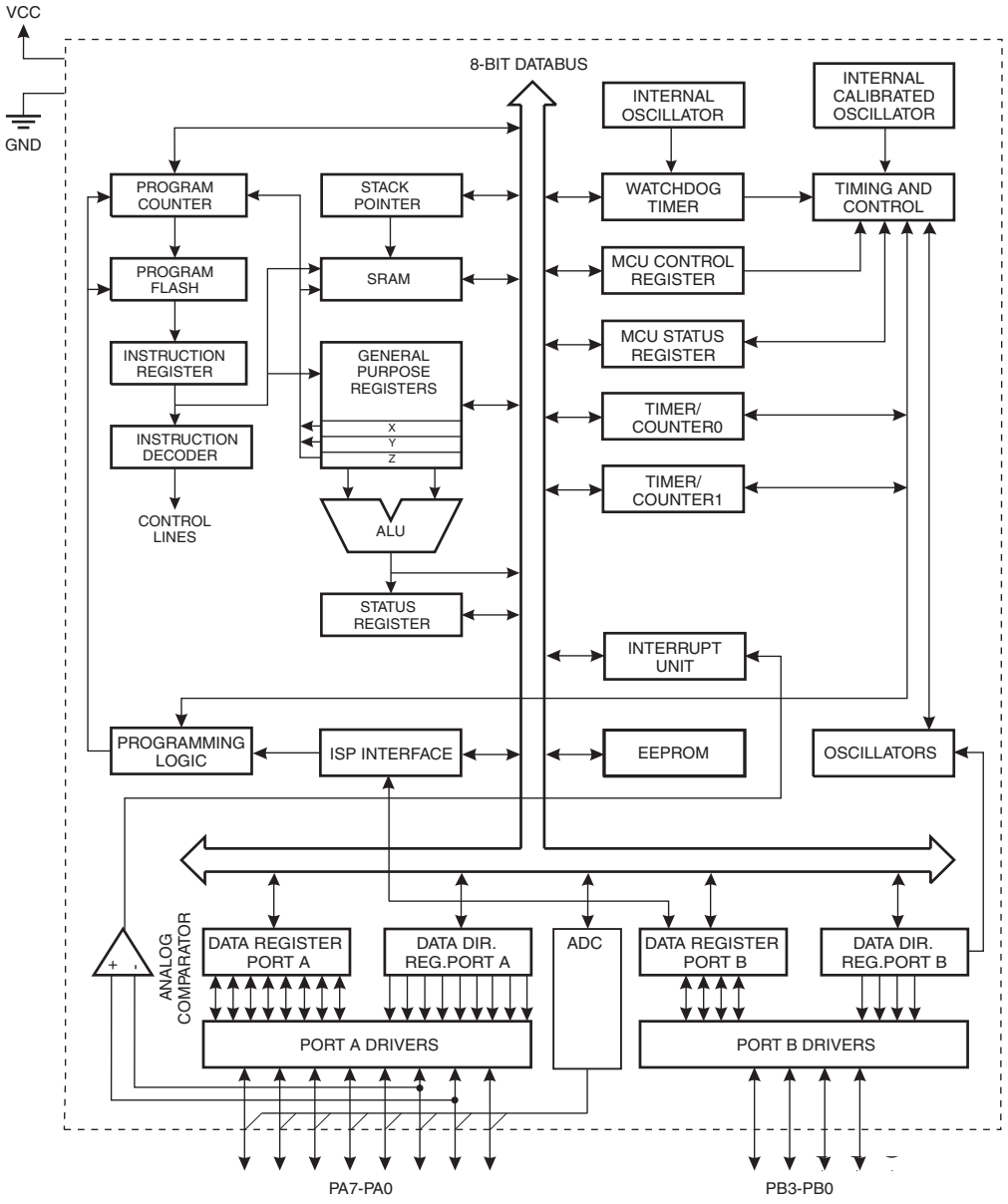
Port A is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A has alternate functions as analog inputs for the ADC, analog comparator, timer/counter, SPI and pin change interrupt.

2. Overview

The ATtiny24/44/84 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny24/44/84 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny24/44/84 provides the following features: 2/4/8K byte of In-System Programmable Flash, 128/256/512 bytes EEPROM, 128/256/512 bytes SRAM, 12 general purpose I/O lines, 32 general purpose working registers, a 8-bit Timer/Counter with two PWM channels, a 16-bit timer/counter with two PWM channels, Internal and External Interrupts, a 8-channel 10-bit ADC, programmable gain stage (1x, 20x) for 12 differential ADC channel pairs, a programmable Watchdog Timer with internal Oscillator, internal calibrated oscillator, and four software selectable power saving modes. Idle mode stops the CPU while allowing the SRAM, Timer/Counter, ADC, Analog Comparator, and Interrupt system to continue functioning. ADC Noise Reduction mode minimizes switching noise during ADC conversions by stopping the CPU and all I/O modules except the ADC. In Power-down mode registers keep their contents and all chip functions are disbaled until the next interrupt or hardware reset. In Standby mode, the crystal/resonator oscillator is running while the rest of the device is sleeping, allowing very fast start-up combined with low power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip ISP Flash allows the Program memory to be re-programmed in-system through an SPI serial interface, by a conventional non-volatile memory programmer or by an on-chip boot code running on the AVR core.

The ATtiny24/44/84 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators and Evaluation kits.

3. About

3.1 Resources

A comprehensive set of drivers, application notes, data sheets and descriptions on development tools are available for download at http://www.atmel.com/avr.

3.2 Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in the extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically, this means “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”. Note that not all AVR devices include an extended I/O map.

3.3 Data Retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

3.4 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

4. Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x3F (0x5F)	SREG	I	T	H	S	V	N	Z	C	
0x3E (0x5E)	SPH	–	–	–	–	–	–	SP9	SP8	
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	
0x3C (0x5C)	OCR0B	Timer/Counter0 – Output Compare Register B								
0x3B (0x5B)	GIMSK	–	INT0	PCIE1	PCIE0	–	–	–	–	
0x3A (0x5A	GIFR	–	INTF0	PCIF1	PCIF0	–	–	–	–	
0x39 (0x59)	TIMSK0	–	–	–	–	–	OCIE0B	OCIE0A	TOIE0	
0x38 (0x58)	TIFR0		–	–	–	–	OCF0B	OCF0A	TOV0	
0x37 (0x57)	SPMCSR	–	–	–	CTPB	RFLB	PGWRT	PGERS	SPMEN	
0x36 (0x56)	OCR0A	Timer/Counter0 – Output Compare Register A								
0x35 (0x55)	MCUCR	BODS	PUD	SE	SM1	SM0	BODSE	ISC01	ISC00	
0x34 (0x54)	MCUSR	–	–	–	–	WDRF	BORF	EXTRF	PORF	
0x33 (0x53)	TCCR0B	FOC0A	FOC0B	–	–	WGM02	CS02	CS01	CS00	
0x32 (0x52)	TCNT0	Timer/Counter0								
0x31 (0x51)	OSCCAL	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	
0x30 (0x50)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	–		WGM01	WGM00	
0x2F (0x4F)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–		WGM11	WGM10	
0x2E (0x4E)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	
0x2D (0x4D)	TCNT1H	Timer/Counter1 – Counter Register High Byte								
0x2C (0x4C)	TCNT1L	Timer/Counter1 – Counter Register Low Byte								
0x2B (0x4B)	OCR1AH	Timer/Counter1 – Compare Register A High Byte								
0x2A (0x4A)	OCR1AL	Timer/Counter1 – Compare Register A Low Byte								
0x29 (0x49)	OCR1BH	Timer/Counter1 – Compare Register B High Byte								
0x28 (0x48)	OCR1BL	Timer/Counter1 – Compare Register B Low Byte								
0x27 (0x47)	DWDR	DWDR[7:0]								
0x26 (0x46)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	
0x25 (0x45)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								
0x24 (0x44)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	–	PSR10	
0x22 (0x42)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	
0x21 (0x41)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0	
0x20 (0x40)	PCMSK1	–	–	–	–	PCINT11	PCINT10	PCINT9	PCINT8	
0x1F (0x3F)	EEARH	–	–	–	–	–	–	–	EEAR8	
0x1E (0x3E)	EEARL	EEAR7	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	
0x1D (0x3D)	EEDR	EEPROM Data Register								
0x1C (0x3C)	EECR	–	–	EEPM1	EEPM0	EERIE	EEMPE	EEPE	EERE	
0x1B (0x3B)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	
0x1A (0x3A)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	
0x19 (0x39)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	
0x18 (0x38)	PORTB	–	–	–	–	PORTB3	PORTB2	PORTB1	PORTB0	
0x17 (0x37)	DDRB	–	–	–	–	DDB3	DDB2	DDB1	DDB0	
0x16 (0x36)	PINB	–	–	–	–	PINB3	PINB2	PINB1	PINB0	
0x15 (0x35)	GPIOR2	General Purpose I/O Register 2								
0x14 (0x34)	GPIOR1	General Purpose I/O Register 1								
0x13 (0x33)	GPIOR0	General Purpose I/O Register 0								
0x12 (0x32)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	
0x11 (0x31))	Reserved	–								
0x10 (0x30)	USIBR	USI Buffer Register								
0x0F (0x2F)	USIDR	USI Data Register								
0x0E (0x2E)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	
0x0D (0x2D)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	
0x0C (0x2C)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	
0x0B (0x2B)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	
0x0A (0x2A)	Reserved	–								
0x09 (0x29)	Reserved	–								
0x08 (0x28)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	
0x07 (0x27)	ADMUX	REFS1	REFS0	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0	
0x06 (0x26)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	
0x05 (0x25)	ADCH	ADC Data Register High Byte								
0x04 (0x24)	ADCL	ADC Data Register Low Byte								
0x03 (0x23)	ADCSRB	BIN	ACME	–	ADLAR	–	ADTS2	ADTS1	ADTS0	
0x02 (0x22)	Reserved	–								
0x01 (0x21)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	
0x00 (0x20)	PRR	–	–	–	–	PRTIM1	PRTIM0	PRUSI	PRADC	

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operation the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

5. Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(z) ← R1:R0	None	
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/Timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

6.1 ATtiny24

Speed (MHz)	Power Supply	Ordering Code[1]	Package[2]	Operational Range
10	1.8 - 5.5V	ATtiny24V-10SSU ATtiny24V-10PU ATtiny24V-10MU	14S1 14P3 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny24-20SSU ATtiny24-20PU ATtiny24-20MU	14S1 14P3 20M1	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.2 ATtiny44

Speed (MHz)	Power Supply	Ordering Code[1]	Package[2]	Operational Range
10	1.8 - 5.5V	ATtiny44V-10SSU ATtiny44V-10PU ATtiny44V-10MU	14S1 14P3 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny44-20SSU ATtiny44-20PU ATtiny44-20MU	14S1 14P3 20M1	Industrial (-40°C to 85°C)

Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

6.3 ATtiny84

Speed (MHz)	Power Supply	Ordering Code[1]	Package[2]	Operational Range
10	1.8 - 5.5V	ATtiny84V-10SSU ATtiny84V-10PU ATtiny84V-10MU	14S1 14P3 20M1	Industrial (-40°C to 85°C)
20	2.7 - 5.5V	ATtiny84-20SSU ATtiny84-20PU ATtiny84-20MU	14S1 14P3 20M1	Industrial (-40°C to 85°C)

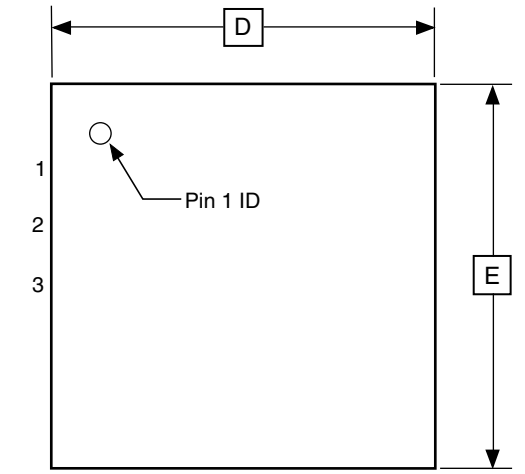
Notes: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

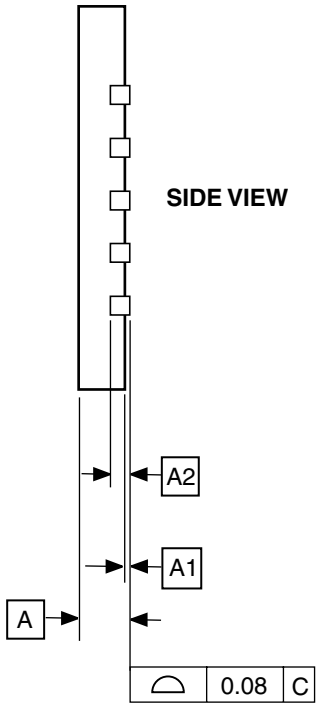
Package Type	
14S1	14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)
14P3	14-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20M1	20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

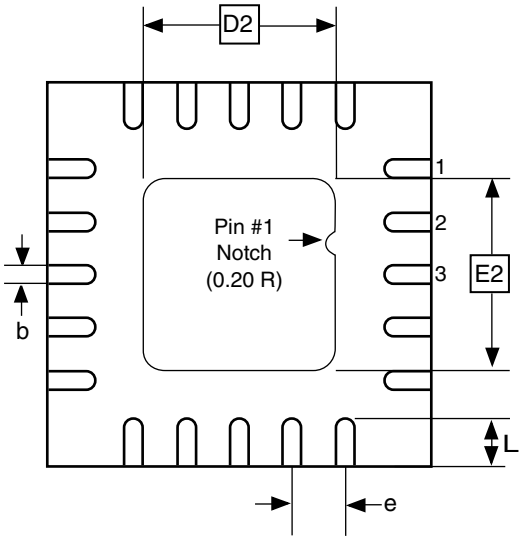
7. Packaging Information

7.1 20M1



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

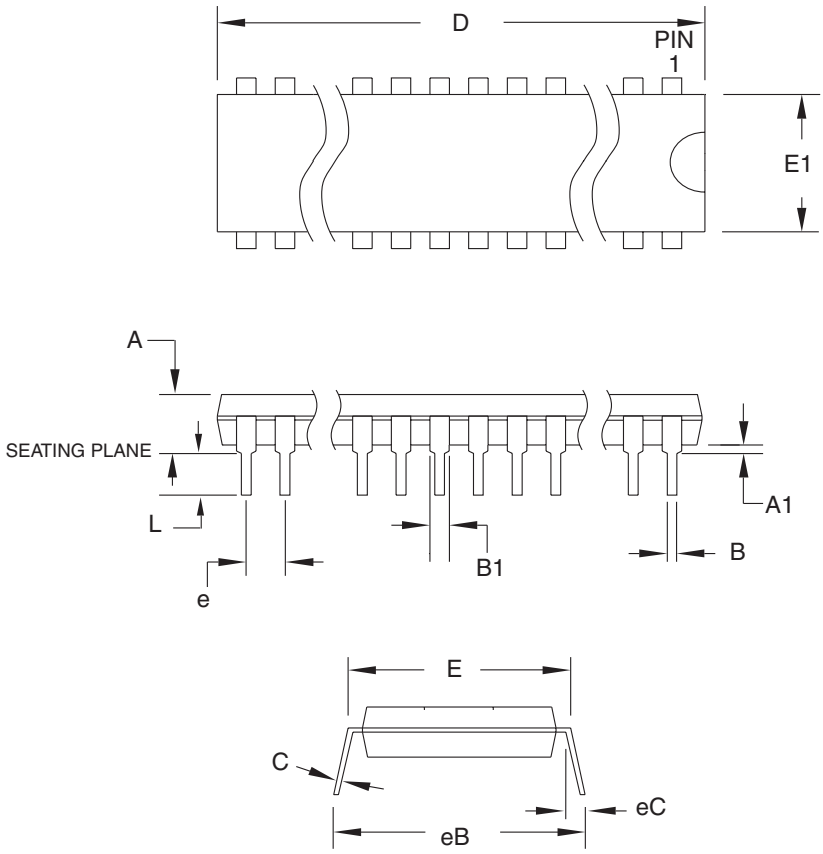
SYMBOL	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	–	0.01	0.05	
A2		0.20 REF		
b	0.18	0.23	0.30	
D		4.00 BSC		
D2	2.45	2.60	2.75	
E		4.00 BSC		
E2	2.45	2.60	2.75	
e		0.50 BSC		
L	0.35	0.40	0.55	

Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

10/27/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20M1**, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm, 2.6 mm Exposed Pad, Micro Lead Frame Package (MLF)	20M1	A

7.2 14P3



COMMON DIMENSIONS
(Unit of Measure = mm)

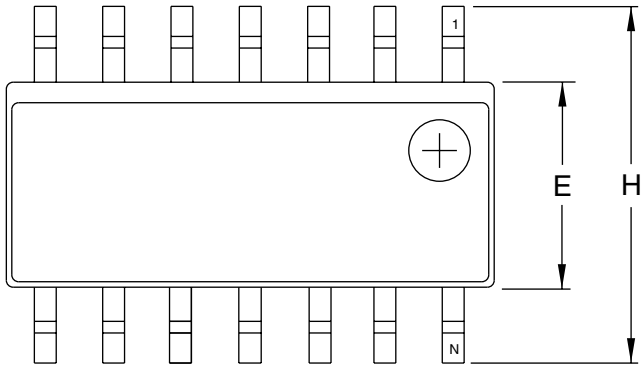
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	18.669	–	19.685	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.143	–	1.778	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AA.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

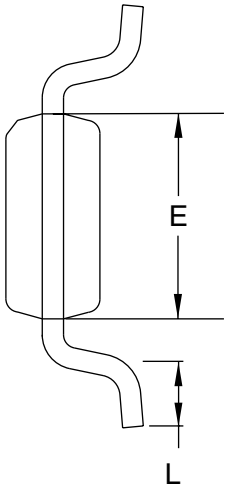
11/02/05

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**14P3**, 14-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	14P3	A

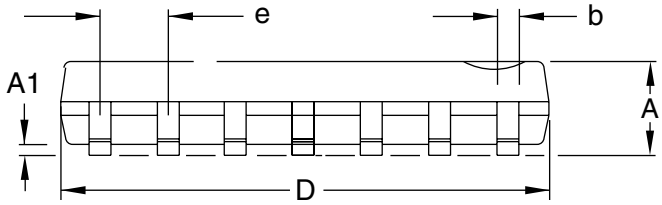
7.3 14S1



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = mm/inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35/0.0532	–	1.75/0.0688	
A1	0.1/.0040	–	0.25/0.0098	
b	0.33/0.0130	–	0.5/0.0200 5	
D	8.55/0.3367	–	8.74/0.3444	2
E	3.8/0.1497	–	3.99/0.1574	3
H	5.8/0.2284	–	6.19/0.2440	
L	0.41/0.0160	–	1.27/0.0500	4
e	1.27/0.050 BSC			

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-012, Variation AB for additional information.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusion and gate burrs shall not exceed 0.15 mm (0.006") per side.
3. Dimension E does not include inter-lead Flash or protrusion. Inter-lead flash and protrusions shall not exceed 0.25 mm (0.010") per side.
4. L is the length of the terminal for soldering to a substrate.
5. The lead width B, as measured 0.36 mm (0.014") or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024") per side.

2/5/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**14S1**, 14-lead, 0.150" Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	14S1	A

8. Errata

The revision letters in this section refer to the revision of the corresponding ATtiny24/44/84 device.

8.1 ATtiny24

8.1.1 Rev. E

No known errata.

8.1.2 Rev. D

No known errata.

8.1.3 Rev. C

- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **Reading EEPROM when system clock frequency is below 900 kHz may not work**
   Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

   Problem Fix/Work around
   Avoid using the EEPROM at clock frequency below 900 kHz.

8.1.4 Rev. B

- **EEPROM read from application code does not work in Lock Bit Mode 3**
- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **EEPROM read from application code does not work in Lock Bit Mode 3**
   When the Memory Lock Bits LB2 and LB1 are programmed to mode 3, EEPROM read does not work from the application code.

   Problem Fix/Work around
   Do not set Lock Bit Protection Mode 3 when the application code needs to read from EEPROM.

2. **Reading EEPROM when system clock frequency is below 900 kHz may not work**
   Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

   Problem Fix/Work around
   Avoid using the EEPROM at clock frequency below 900 kHz.

8.1.5 Rev. A

Not sampled.

8.2 ATtiny44

8.2.1 Rev. D

No known errata.

8.2.2 Rev. C

No known errata.

8.2.3 Rev. B

No known errata.

8.2.4 Rev. A

- **Reading EEPROM when system clock frequency is below 900 kHz may not work**

1. **Reading EEPROM when system clock frequency is below 900 kHz may not work**
   Reading data from the EEPROM at system clock frequency below 900 kHz may result in wrong data read.

   Problem Fix/Work around
   Avoid using the EEPROM at clock frequency below 900 kHz.

8.3 ATtiny84

8.3.1 Rev. B

No known errata.

8.3.2 Rev. A

No known errata.

9. Datasheet Revision History

9.1 Rev G. 01/08

1. Updated sections:
   – “Features” on page 1
   – “RESET” on page 3
   – “Overview” on page 4
   – “About” on page 6
   – “SPH and SPL — Stack Pointer Register” on page 11
   – “Atomic Byte Programming” on page 17
   – “Write” on page 17
   – “Clock Sources” on page 24
   – “Default Clock Source” on page 28
   – “Sleep Modes” on page 32
   – “Software BOD Disable” on page 33
   – “External Interrupts” on page 48
   – “USIBR – USI Data Buffer” on page 124
   – “USIDR – USI Data Register” on page 124
   – “DIDR0 – Digital Input Disable Register 0” on page 131
   – “Features” on page 132
   – “Prescaling and Conversion Timing” on page 135
   – “Temperature Measurement” on page 144
   – “ADMUX – ADC Multiplexer Selection Register” on page 145
   – “Limitations of debugWIRE” on page 152
   – “Reading Lock, Fuse and Signature Data from Software” on page 155
   – “Device Signature Imprint Table” on page 161
   – “Enter High-voltage Serial Programming Mode” on page 168
   – “Absolute Maximum Ratings*” on page 175
   – “DC Characteristics” on page 175
   – “Speed Grades” on page 177
   – “Clock Characteristics” on page 177
   – “Calibrated Internal RC Oscillator Accuracy” on page 177
   – “System and Reset Characteristics” on page 179
   – “Supply Current of I/O Modules” on page 186
   – “ATtiny24” on page 17
   – “ATtiny44” on page 18
   – “ATtiny84” on page 19
2. Updated bit definitions in sections:
   – “MCUCR – MCU Control Register” on page 35
   – “MCUCR – MCU Control Register” on page 50
   – “MCUCR – MCU Control Register” on page 66

– “PINA – Port A Input Pins” on page 67
– “SPMCSR – Store Program Memory Control and Status Register” on page 157
– “Register Summary” on page 7

3. Updated Figures:
   – “Reset Logic” on page 38
   – “Watchdog Reset During Operation” on page 41
   – “Compare Match Output Unit, Schematic (non-PWM Mode)” on page 97
   – “Analog to Digital Converter Block Schematic” on page 133
   – “ADC Timing Diagram, Free Running Conversion” on page 137
   – “Analog Input Circuitry” on page 140
   – “High-voltage Serial Programming” on page 167
   – “Serial Programming Timing” on page 184
   – “High-voltage Serial Programming Timing” on page 185
   – “Active Supply Current vs. Low Frequency (0.1 - 1.0 MHz)” on page 187
   – “Active Supply Current vs. frequency (1 - 20 MHz)” on page 188
   – “Active Supply Current vs. VCC (Internal RC Oscillator, 8 MHz)” on page 188
   – “Active Supply Current vs. VCC (Internal RC Oscillator, 1 MHz)” on page 189
   – “Active Supply Current vs. VCC (Internal RC Oscillator, 128 kHz)” on page 189
   – “Idle Supply Current vs. Low Frequency (0.1 - 1.0 MHz)” on page 190
   – “Idle Supply Current vs. Frequency (1 - 20 MHz)” on page 190
   – “Idle Supply Current vs. VCC (Internal RC Oscillator, 8 MHz)” on page 191
   – “Idle Supply Current vs. VCC (Internal RC Oscillator, 1 MHz)” on page 191
   – “Idle Supply Current vs. VCC (Internal RC Oscillator, 128 MHz)” on page 192
   – “Power-down Supply Current vs. VCC (Watchdog Timer Disabled)” on page 192
   – “Power-down Supply Current vs. VCC (Watchdog Timer Enabled)” on page 193
   – “Reset Pin Input Hysteresis vs. VCC” on page 203
   – “Reset Pin Input Hysteresis vs. VCC (Reset Pin Used as I/O)” on page 204
   – “Watchdog Oscillator Frequency vs. VCC” on page 206
   – “Watchdog Oscillator Frequency vs. Temperature” on page 206
   – “Calibrated 8 MHz RC Oscillator Frequency vs. VCC” on page 207
   – “Calibrated 8 MHz RC oscillator Frequency vs. Temperature” on page 207
   – “ADC Current vs. VCC” on page 208
   – “Programming Current vs. VCC (ATtiny24)” on page 210
   – “Programming Current vs. VCC (ATtiny44)” on page 210
   – “Programming Current vs. VCC (ATtiny84)” on page 211
4. Added Figures:
   – “Reset Pin Output Voltage vs. Sink Current (VCC = 3V)” on page 199
   – “Reset Pin Output Voltage vs. Sink Current (VCC = 5V)” on page 199
   – “Reset Pin Output Voltage vs. Source Current (VCC = 3V)” on page 200
   – “Reset Pin Output Voltage vs. Source Current (VCC = 5V)” on page 200
5. Updated Tables:

- “Device Clocking Options Select” on page 24
- “Start-up Times for the Crystal Oscillator Clock Selection” on page 28
- “Start-up Times for the Internal Calibrated RC Oscillator Clock Selection” on page 26
- “Start-up Times for the External Clock Selection” on page 25
- “Start-up Times for the 128 kHz Internal Oscillator” on page 26
- “Active Clock Domains and Wake-up Sources in the Different Sleep Modes” on page 32
- “Watchdog Timer Prescale Select” on page 46
- “Reset and Interrupt Vectors” on page 47
- “Overriding Signals for Alternate Functions in PA7..PA5” on page 62
- “Overriding Signals for Alternate Functions in PA4..PA2” on page 63
- “Overriding Signals for Alternate Functions in PA1..PA0” on page 63
- “Port B Pins Alternate Functions” on page 64
- “Overriding Signals for Alternate Functions in PB3..PB2” on page 65
- “Overriding Signals for Alternate Functions in PB1..PB0” on page 66
- “Waveform Generation Modes” on page 109
- “ADC Conversion Time” on page 138
- “Temperature vs. Sensor Output Voltage (Typical Case)” on page 144
- “DC Characteristics. TA = -40×C to +85×C (1)” on page 175
- “Calibration Accuracy of Internal RC Oscillator” on page 178
- “Reset, Brown-out, and Internal Voltage Characteristics” on page 179
- “VBOT vs. BODLEVEL Fuse Coding” on page 180
- “ADC Characteristics, Single Ended Channels. -40×C - 85×C” on page 181
- “ADC Characteristics, Differential Channels (Bipolar Mode), TA = -40×C to 85×C” on page 183
- “Serial Programming Characteristics, TA = -40×C to 85×C, VCC = 1.8 - 5.5V (Unless Otherwise Noted)” on page 184
- “High-voltage Serial Programming Characteristics TA = 25×C, VCC = 5V (Unless otherwise noted)” on page 185

6. Updated code examples in sections:
   - “Write” on page 17
   - “SPI Master Operation Example” on page 119
7. Updated “Ordering Information” in
   - “ATtiny84” on page 13

9.2 Rev F. 02/07

1. Updated Figure 1-1 on page 2, Figure 8-7 on page 42, Figure 20-6 on page 185.
2. Updated Table 9-1 on page 47, Table 10-7 on page 64, Table 11-2 on page 79, Table 11-3 on page 80, Table 11-5 on page 80, Table 11-6 on page 81, Table 11-7 on page 81, Table 11-8 on page 82, Table 20-10 on page 183, Table 20-12 on page 185.
3. Updated table references in “TCCR0A – Timer/Counter Control Register A” on page 79.

4. Updated Port B, Bit 0 functions in “Alternate Functions of Port B” on page 64.
5. Updated WDTCR bit name to WDTCSR in assembly code examples.
6. Updated bit5 name in “TIFR1 – Timer/Counter Interrupt Flag Register 1” on page 113.
7. Updated bit5 in “TIFR1 – Timer/Counter Interrupt Flag Register 1” on page 113.
8. Updated “SPI Master Operation Example” on page 119.
9. Updated step 5 in “Enter High-voltage Serial Programming Mode” on page 168.

9.3 Rev E. 09/06

1. All characterization data moved to “Electrical Characteristics” on page 175.
2. All Register Descriptions gathered up in separate sections at the end of each chapter.
3. Updated “System Control and Reset” on page 38.
4. Updated Table 11-3 on page 80, Table 11-6 on page 81, Table 11-8 on page 82, Table 12-3 on page 108 and Table 12-5 on page 109.
5. Updated “Fast PWM Mode” on page 99.
6. Updated Figure 12-7 on page 100 and Figure 16-1 on page 133.
7. Updated “Analog Comparator Multiplexed Input” on page 129.
8. Added note in Table 19-12 on page 165.
9. Updated “Electrical Characteristics” on page 175.
10. Updated “Typical Characteristics” on page 186.

9.4 Rev D. 08/06

1. Updated “Calibrated Internal 8 MHz Oscillator” on page 25.
2. Updated “OSCCAL – Oscillator Calibration Register” on page 29.
3. Added Table 20-2 on page 178.
4. Updated code examples in “SPI Master Operation Example” on page 119.
5. Updated code examples in “SPI Slave Operation Example” on page 120.
6. Updated “Signature Bytes” on page 162.

9.5 Rev C. 07/06

1. Updated Features in “USI – Universal Serial Interface” on page 117.
2. Added “Clock speed considerations” on page 123.
3. Updated Bit description in “ADMUX – ADC Multiplexer Selection Register” on page 145.
4. Added note to Table 18-1 on page 157.

9.6 Rev B. 05/06

1. Updated “Default Clock Source” on page 28
2. Updated “Power Reduction Register” on page 34.
3. Updated Table 20-4 on page 179, Table 9-4 on page 42, Table 16-3 on page 145, Table 19-5 on page 161, Table 19-12 on page 165, Table 19-16 on page 172, Table 20-10 on page 183.
4. Updated Features in “Analog to Digital Converter” on page 132.

5. Updated Operation in “Analog to Digital Converter” on page 132.
6. Updated “Temperature Measurement” on page 144.
7. Updated DC Characteristics in “Electrical Characteristics” on page 175.
8. Updated “Typical Characteristics” on page 186.
9. Updated “Errata” on page 17.

9.7 Rev A. 12/05

Initial revision.

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